

Abstract of the Disclosure

An integrated circuit die and method of fabricating the same. The method comprises further grinding, polishing or otherwise treating one or more perimeter edges of an individual circuit die. The perimeter edges are treated to remove a substantial portion of the remaining substrate material layer or scribe therefrom without exposing the active circuitry of the die. The process reduces the overall length and width dimensions of a die producing a smaller circuit die without reducing the amount of circuitry on the die.

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